Remarks

The Office Action dated April 27, 2009 notes that the finality of the previous office action has been withdrawn and the following rejections: claims 1-4, 6, 8 and 12 stand rejected under 35 U.S.C. § 102(b) over Krakauer (U.S. Patent No. 5,617,283); claims 1-3 and 11 stand rejected under 35 U.S.C. § 102(b) over John (U.S. Patent No. 6,522,511); claims 5 and 7 stand rejected under 35 U.S.C. § 103(a) over the '283 reference; claim 10 stands rejected under 35 U.S.C. § 103(a) over the '283 reference in view of Ker (U.S. Patent Pub. 2002/0050615); claims 11 and 15 stand rejected under 35 U.S.C. § 103(a) over the '283 reference in view of Lai (US Patent Pub. 2003/0235022); and claims 12-15 stand rejected under 35 U.S.C. § 103(a) over the '511 reference in view of Avery (U.S. Patent No. 6,501,632). The Specification is objected to due to informalities. Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

At the outset Applicant notes that claim 9 has not been rejected with the explanation at paragraph three (p. 2) of the Office Action. Applicant requests clarification whether the intent was to reject claim 9 or to allow it.

Regarding the objection to the Specification, Applicant disagrees that no explanation/support of the time delay circuit has been provided and/or is required. In connection with Figure 2, the time delay circuit is described as including R and MN1, which provide drive current to the node NET1 as fast as possible. See the tables before the claim section.

Applicant respectfully traverses the § 102(b) and § 103(a) rejections because the cited Krakauer '283 and John '511 references either alone or in combination with the other cited reference lacks correspondence to the claimed invention. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.*, a time-delay circuit that includes a resistor and a capacitive device connected in series between a power supply and control inputs of first and second transistors. Because none of the cited references teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejections fail.

More specifically, Applicant respectfully submits that the rejections rely upon an interpretation that is inconsistent with the teachings of the references and Applicant's specification and that is contrary to how the skilled artisan would interpret the limitations in violation of M.P.E.P. § 2111. The unreasonableness of the Examiner's interpretation is highlighted by the attempt to assert that a wire connection (assumed by the teachings to have effectively zero resistance) functions as resistive component of a time-delay circuit (*see, e.g.*, the interpretation of claim 12 on page 3 of the instant Office Action). In pertinent part, the Examiner is of the opinion that a connection wire is functioning to provide a resistive function of the time-delay circuit. Applicant submits that the skilled artisan understands that the resistance in a circuit wire is assumed to be zero, particularly for an RC time-delay circuit, unless expressly discussed otherwise. To assert otherwise is contrary to Applicant's Specification, the teachings of the cited references and the general terminology and understanding of the skilled artisan.

The skilled artisan would understand that there is only a *de minimis* resistance, capacitance and inductance in all circuits. Applicant submits that for an expressly discussed circuit element the skilled artisan assumes that a resistive, capacitive or inductive value is significantly more than *de minimis*. Both the cited references and Applicant's specification are consistent with this conventional use of terminology. Applicant requests that the Examiner consider the consequences of using such overly-broad and unreasonable interpretations. Using the Examiner's logic, the validity of a huge volume of applied-for and issued patent claims would be called into question.

Applicant previously highlighted the impropriety of the Examiner's assertion that wire connections correspond to the separate circuit elements (*e.g.,* resistors and capacitors as claimed), to which the Examiner failed to adequately respond as required by M.P.E.P. § 707.07(f). The Examiner's response in the instant Office Action does not address the fact that the Examiner's assertions of correspondence violate M.P.E.P. § 2111 (as discussed in detail by Applicant in the instant and previous Responses). Thus, the record is clear that the Examiner's assertion that wire connections correspond to separate resistive and capacitive elements is improper. The following discussion particularly addresses the impropriety of each of the rejections.

Applicant respectfully traverses the § 102(b) and § 103(a) rejections based on the '283 reference because the cited portions of the '283 reference do not correspond to aspects of the claimed invention directed to a time-delay circuit that includes a resistor and a capacitive device connected in series between a power supply and control inputs of first and second transistors. The Examiner erroneously asserts that the "connection means" between transistor 42 (*i.e.,* the asserted capacitive device) and signal line 16 (*i.e.,* the asserted power supply) correspond to Applicant's resistor. The Examiner's assertion of correspondence violates M.P.E.P. § 2111, which requires that the claims be given their broadest reasonable construction in light of Applicant's specification as it would be interpreted by one of ordinary skill in the art. Applicant submits that simply because "connection means" (*e.g.,* wires) have some (nominal) resistance does not mean that the skilled artisan would interpret a wire as corresponding to a resistor. The skilled artisan, in view of Applicant's specification (*see, e.g.,* Figure 2 and paragraph 0034), would interpret the resistor of the claimed invention as being an element that effects the operation of a circuit, in contrast to the "connection means," which have a nominal impact on the operation of the circuit. As such, the skilled artisan, in view of Applicant's specification, would not interpret the "connection means" of the '283 reference as being a resistor. Accordingly, the Examiner's interpretation of the claimed invention violates M.P.E.P. § 2111.

Moreover, the cited portions of the '283 reference do not teach that transistor 42 (*i.e.,* the asserted capacitive device) is connected to a power supply, and, in fact, the '283 reference teaches away from connecting transistor 42 to a power supply. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('283) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). The cited teachings of the '283 reference indicate that transistor 42 is connected to signal line 16. In fact, the '283 reference teaches that the embodiment disclosed in Figure 2 eliminates the need for a reference supply voltage (*e.g.,* V_{DD}) to be available for the modulation circuit 40. *See, e.g.*, Col. 4:59-67. As such, the

'283 reference teaches away from connecting transistor 42 to a power supply. Applicant previously highlighted the fact that the '283 reference teaches away from connecting transistor 42 to a power supply, to which the Examiner failed to respond in any manner as required by M.P.E.P. § 707.07(f).

In view of the above, the § 102(b) and § 103(a) rejections based on the '283 reference are improper and Applicant requests that they be withdrawn.

Applicant respectfully traverses the § 102(b) rejection based on the '511 reference because the cited portions of the '511 reference do not correspond to aspects of the claimed invention directed to a time-delay circuit that includes a resistor and a capacitance device connected in series between a supply voltage terminal and control inputs of first and second transistors. The Examiner once again improperly asserts that "connection means" in a circuit correspond to a separate circuit element, specifically, that "the line capacitance of the connection means of R of 30 in Figure 3" corresponds to Applicant's capacitive device. The Examiner's interpretation of the claimed invention essentially gives no meaning to the claimed capacitive device and, as discussed above, such an interpretation violates M.P.E.P. § 2111 (The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art."). Accordingly, the § 102(b) rejection based on the '511 reference is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejections based on the '511 reference because the cited combination does not correspond to aspects of the claimed invention directed to a time-delay circuit that includes a resistor and a capacitive device connected in series between a power supply and control inputs of first and second transistors. The Examiner acknowledges that the '511 reference does not teach or suggest a time-delay circuit connected as in the claimed invention. The Examiner then erroneously asserts that the '632 reference teaches that resistor R_{Z1} and capacitor C are connected in series between pad 301 and the control input of the NMOS transistor. *See, e.g.,* Figure 3. In actuality, the '632 reference teaches that resistor R_{Z1} is the internal (or parasitic) resistance of Zener diode Z1, and that an alternative to using Zener diode Z1 is to use capacitor C (shown in phantom

in Figure 3) in lieu of the diode Z1. *See, e.g.,* Col. 3:5-6 and Col. 3:56-61. Thus, the '632 reference teaches that either Zener diode Z1 (*i.e.,* resistor R_{Z1}) or capacitor C is connected between pad 302 and the control input of the NMOS transistor, not both. The Examiner has now twice continued to assert that the '632 reference "teaches that Z1 can be replaced by a capacitance, to result in Rz1 and C in series." However, the Examiner's position is directly contradicted by the express teachings of the '632 reference, which state that the resistor R_{Z1} is the internal resistance of diode Z1 and thus resistor R_{Z1} is no longer present in the circuit of Figure 3 when the diode Z1 is replaced by capacitor C. Applicant respectfully requests that the Examiner review the '632 reference since even a cursory examination of the '632 reference would identify the impropriety of the Examiner's position. As such, the § 103(a) rejection of claims 12-15 fails to establish *prima facie* obviousness, based upon the lack of teaching or suggestion of all limitations.

Moreover, the '511 reference expressly teaches away from the asserted combination with the '632 reference. *See, e.g., KSR* discussed above. Specifically, the '511 reference expressly teaches that a capacitive device should not be used (*see, e.g.*, Col. 2:14-17). In addition, this is one of the primary objects of the '511 reference and the proposed modification would render the circuit of the '511 reference unsuitable for use in high-speed digital circuitry. *See, e.g.,* M.P.E.P. § 2143.01 ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."). Applicant previously highlighted the impropriety of the Examiner's proposed combination of the '511 and '632 references, to which the Examiner failed to respond in any manner as required by M.P.E.P. § 707.07(f). Accordingly, the § 103(a) rejections based on the '511 reference are improper and Applicant requests that they be withdrawn.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____
Robert J. Crawford
Reg. No.: 32,122
(NXPS.446PA)